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ESD Protection Design and Characteristic Analysis of Advanced Process Integrated Circuit

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Abstract

The electrostatic discharge (ESD) phenomenon is very common, in daily life, many places will appear ESD phenomenon. However, ESD is a potential hazard for integrated circuits. This paper analyzes the ESD protection design and characteristics of advanced process integrated circuits, and puts forward personal views combined with experience, hoping to bring help to the people who pay attention to the ESD protection of integrated circuits.

Keywords: Electrostatic Protection; Integrated Circuit; Failure Analysis

INTRODUCTION

with the development of science and technology, the quality of integrated circuit is improving, while the volume is becoming smaller and smaller. However, in the operation process of integrated circuit, high-voltage ESD will bring high-density current, which may lead to insulator breakdown and bring hidden danger to the operation of integrated circuit. Therefore, it is necessary to analyze the ESD protection design and characteristics of advanced process integrated circuits.

1 ESD PROTECTION DESIGN OF ADVANCED PROCESS INTEGRATED CIRCUIT

1.1 Esd Protection of Nano Integrated Circuit Chip

In general, the ESD protection on 28nm advanced CMOS process chip needs to meet the following requirements: first, ESD protection has relatively small on resistance, so it can protect the circuit by controlling the voltage when the ESD pulse arrives. Second, protective devices need to have high robustness, which can get higher protection level with smaller area and save protection cost. Thirdly, the performance parameters of protective devices can meet the ESD window of 28nm. Fourth, 28nm CMOS process usually works on high-speed chips, so it is necessary to ensure that ESD protection devices can have enough turn-on speed.

1.2 Failure Analysis and Improvement of 28cmos Chip

In order to better study the ESD protection design under 28nm COMS process, it is necessary to carry out a comprehensive failure analysis and carry out systematic research on the 28nm COMS process chip. According to TLP test and other technical means, ESD protection is improved.

In the failure analysis, it is necessary to test the GPIO port ESD and HBM. When the voltage of HBM reaches 4KV, the pin of the chip will fail, and the active area in the internal protection circuit and the surrounding metal wire will be burnt out. When the failure occurs, it is necessary to combine the chip circuit diagram and process layout to locate the specific failure device and the failure location. It is found that the failure location is PMOS and NMOS tubes (Fig. 1 shows the chip circuit and failure location diagram). These two pipe fittings are connected with the output pin and form the inverter structure. When the failure occurs, fuse burning occurs because of the leakage and gate This failure is likely due to the long ESD discharge path and the high on resistance of ESD clamp device, which results in high clamping voltage.

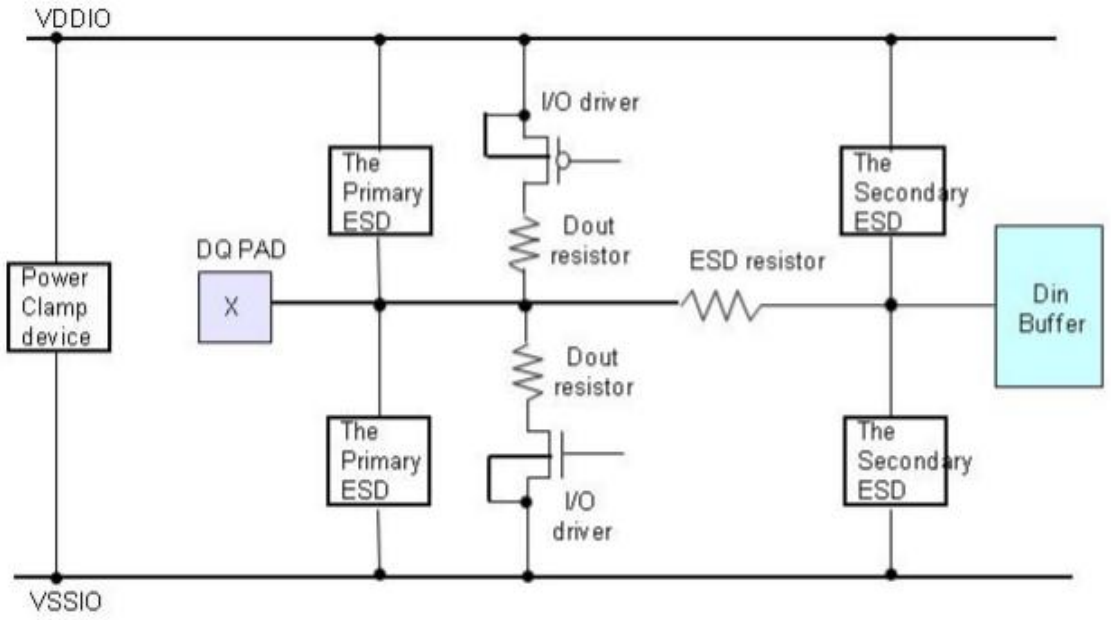

FIGURE 1 CHIP CIRCUIT AND FAILURE LOCATION DIAGRAM

In order to eliminate contingency, more chips need to be tested for HBM, and the final results can also show that the failure position is in the position of PMOS and NOMs. The ESD protection device of GPIO pin is GGNMOS. Through TLP test of GPIO pin, it can be found that TLP curve of chip pin is basically similar. Through TLP test, it can be found that all GPIO ports use the same size of GGNMOS as ESD protection devices. The results show that the trigger voltage is 5.33v, the holding voltage is 4.56v, the failure current is about 2.7A, and the failure current of a single GGNMOS tube is about 3.5A. After failure analysis of the GGNMOS tube, it is found that the ESD protection device GGNMOS tube is not damaged. The damaged tube is NMOS tube and PMOS tube. The chip adopts the 28nm process of TSMC, and the breakdown voltage of MOS gate is 9V It has good protection effect on NMOS tube and PMOS tube. On the contrary, because the on resistance of GGNMOS is too high, the clamping voltage increases continuously, which eventually exceeds the breakdown voltage of NMOS and PMOS, resulting in the burnout of NMOS and PMOS.

In view of the ESD protection problems of the chip, the following design suggestions can be given: first, the clamping capacity of the ESD protection device GGNMOS is relatively poor, and the opening speed is relatively slow. Therefore, the ESD protection problem can be improved by replacing the protective device with relatively small on resistance or by adding low-voltage TVs. Secondly, NMOS and PMOS as output tubes have relatively poor anti wear ability. Therefore, it is necessary to optimize the layout layout of the output tube to improve the breakdown voltage of the tube. Thirdly, the ESD energy outside the chip can be reduced by grounding to improve the electromagnetic compatibility and protection capability of the chip.

1.3 New ESD Protection Structure for SCR

The ESD protection capability of the chip can be significantly improved by mos-scr protective devices. In the design process, the GGNMOS structure can be added to the traditional SCR, so that the GGNMOS tube and SCR are in the same protection device at the same time, Through TCAD simulation, the ESD test and failure analysis can be verified, so as to find out the working principle of the new device. By adjusting various parameters of the protection device, mos-scr protection device can have the low trigger voltage, high maintenance voltage and high robustness of GGNMOS at the same time, so as to improve the ESD protection ability. The curve obtained by TLP test shows that mos-scr has double hysteresis characteristics, so the clamping voltage can be controlled at a relatively low level. In addition, vftlp test also shows that mos-scr device has double hysteresis characteristics at 1a Under tap current, the overshoot voltage is not more than 7V, and its turn-on speed is very fast, and the turn-on time is only 2.3ns. It can be found that the mos-scr device is very suitable for the ESD protection of 28nm CMOS process.

2 POWER CLAMP TIME WINDOW CHARACTERISTICS OF RC NMOS

Power clamp is a network structure that triggers NMOS by RC. The rising edge of ESD waveform is detected to trigger NMOS tube. Therefore, ESD waveform has a great impact on power clamp structure at different times. Simulation of RC NMOS parameters under different ESD waveforms can be completed by cadence spectrum software. According to IEC61000-4-2 EMC test standard, the discharge standard waveform of IEC 2KV is short-circuit current peak current value is 7.5A, the current rise time is 1ns, the current is 4A at 30ns, and the current is 2A at 60ns. Considering the parasitic effect, the discharge model is established. The simulation output waveform and discharge model constructed by cadence spectre software show that the current rise speed is relatively slow, and the time required for current rise will be longer.

The discharge network of IEC to RC NMOS power clamp is constructed by cadence spectre software. Under the same RC time constant, IEC pulse will impact RC The opening time of NMOS can be determined by RC and the size of the tube. The size of the tube is directly proportional to the capacitance, and the size of the NMOS tube is inversely proportional to the on resistance. When the size of the NMOS tube increases, the clamping voltage and residual voltage will be reduced. In order to form a low resistance path in power clamp, NMOS is usually designed as a multi interdigital structure. In addition, IEC discharge simulation of NMOS with the same size under different time constant power clamp is carried out. The simulation results are shown in Table 1. Small RC time constant will lead to insufficient ESD discharge of NMOS. Therefore, it is necessary to ensure the rationality of RC time constant setting.

TABLE 1 CONDUCTION OF NMOS TUBES OF THE SAME SIZE (W = 2000 M M) IN DIFFERENT RC TIME CONSTANTS

RC ns	Residual Voltage V@600nS	Opening situation
100	8	Not open
200	5	Not fully opened 150ns / 350ns
500	1.2	MOS switching time 100ns / 350ns
1000	1	Switch on time 100ns / 420ns
1500	0	open

CONCLUSION

In a word, ESD protection design and characteristic analysis of advanced process integrated circuit are very important, which can significantly improve the ESD protection effect and increase the safety of IC during operation. I believe that as more people pay attention to the ESD protection of integrated circuits, ESD protection design will become more perfect.

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